HIGH VOLTAGE CMOS SWITCH WITH REDUCED HIGH VOLTAGE JUNCTION STRESSES

ABSTRACT

[0044] A high voltage switch circuit is disclosed for reducing high voltage junction stresses. The circuit contains a cascode device structure having one or more transistors of a same type connected in a series and being operable with a normal operating voltage and a high operating voltage. The cascode device structure comprises a high operating voltage coupled to a first end of the device structure, a low voltage coupled to a second end, and one or more control voltages controllably coupled to the gates of the transistors, wherein at least one of the control voltages coupled to the gate of at least one transistor is raised to a medium voltage level that is higher than a normal operating voltage when operating under the high operating voltage for tolerating stress imposed thereon by the high operating voltage.

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